REMARKS

By this Response, claims 15 and 16 have been amended and the rejection of claims 1-14 has been traversed. Claims 1-16 of this application are pending. Reconsideration of this application and allowance of all pending claims are hereby respectfully requested.

Objection under 37 CFR 1.75(c)

The Examiner objected to claims 15 and 16 as being in an improper form because of multiple dependency. By this Amendment, claims 15 and 16 have been amended to remove the multiple dependency. The reconsideration of the allowance of the amended claims is hereby respectfully requested.

Rejection under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-5 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2004/0070440 (Tang et al.). Claims 1-5 and 13-14 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,682,118 (Kaenal et al.). The Applicants respectfully traverse the rejection.

Tang et al. disclose setting a bias voltage Vbs (local supply voltage Vcc – body voltage Vout') to a pre-determined value in advance and controlling the body voltage Vout' so that the bias voltage Vbs can be fixed at the pre-determined value when the local supply voltage Vcc fluctuates. According to Tang et al., when the bias voltage Vbs is kept at the pre-determined value, a threshold voltage is also kept at a value corresponding to the bias voltage Vbs. To maintain the threshold voltage at a constant level, a saturation current value Ids of the MOS transistors varies in accordance with the change occurred in the supply voltage Vdd (Vcc) based on certain known relationship. Therefore, according to Tang et al., a body voltage Vout'

(substrate voltage) is controlled so that the bias voltage Vbs remains at a pre-determined value when the local supply voltage Vdd changes. Due to this control scheme, the saturation current value changes with the local supply voltage Vdd.

The teaching in the present application is completely different from what Tang et al. teach. According to the teaching of the present application, when a supply voltage Vdd varies, at a threshold voltage, the saturation current value Ids of the MOS transistors is made to reach a pre-determined constant value and the substrate voltage is controlled to obtain such a threshold voltage. The present invention teaches a body voltage Vout' (substrate voltage) is controlled so that the saturation current value Ids of the MOS transistors remains at a pre-determined (constant) value, as recited in independent claim 1 and 13 ("an actual saturation current value of the MOS transistor given the operating power supply voltage value of the main circuit is equal to the target saturation current value").

It is well-settled that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Since Tang et al. do not teach or suggest controlling the substrate potential of the MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor given the operating power supply voltage value of the main circuit is equal to the target saturation current value, as recited in claim 1, or controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value, as recited in claim 13, the Applicants respectfully submit that Tang et al. do not anticipate claim 1 or claim 13.

Kaenel et al. disclose detecting a current flowing into a main circuit (119) by a resistor RS and an amplifier (125) and sending the detected current back to current sources (111 and 118 in Fig. 7). As a result, the amount of current flowing out from the current sources increases when the amount of the detected current is large (i.e., when a supply voltage Vlog is low). When the amount of current flowing out from the current sources increases, circuits 105 – 107 and 112-114 control the bias voltages VBN and VBP of transistors 109 and 116 to high so that the threshold voltages of the transistors 109 and 116 is driven to low. The circuits operate oppositely when the amount of current flowing into the main circuit 119 is detected to be small. According to the teaching of Kaenel et al., the reduced-voltage source 104 receives the bias voltages VBN and VBP, which are output voltages of control circuits 101 and 102, respectively, and a supply voltage Vlog is generated based on the bias voltage (substrate voltages) VBN and VBP. Consequently, the saturation current (i.e., the current flowing from the current sources 111 and 118 to the transistors 109 and 116) increases or decreases in accordance with the amount of current detected by the resistor RS or in accordance with the change in the supply voltage Vlog.

The teaching in the present application is different from Kaenal. The substrate voltage is fixed or controlled and the supply voltage Vdd is controlled independent of the substrate voltage so that the saturation current flowing into the transistors 109 and 116 remains at a pre-determined constant value, as recited in independent claim 1 and 13 ("an actual saturation current value of the MOS transistor given the operating power supply voltage value of the main circuit is equal to the target saturation current value"). At a minimum, Kaenel et al. fail to teaching this feature and the Applicants respectfully submit that Kaenel et al. do not anticipate claim 1 or claim 13. Since neither Tang et al. nor Kaenel et al. anticipates claims 1 and 13, the

Applicants respectfully request that the 102 rejections of claims 1 and 13 based on Tang et al. or Kaenel et al. be withdrawn.

Claims 2-5 depend from claim 1. Therefore, claims 2-5 are patentable at least for the reasons stated above with respect to claim 1 and for the additional features recited therein.

Similarly, claim 14 depends from claim 13. Therefore, claim 14 is patentable at least for the reasons stated above with respect to claim 13 and for the additional features recited therein. The Applicants respectfully request that rejection to claims 2-5 and 14 based on anticipation be withdrawn.

Rejection under 35 U.S.C. § 103

Claims 6-9 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang et al. in view of U.S. Patent No. 6,456,157 (Forbes et al.). Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang et al. and Forbes et al. as applied to claims 6-9 above, and further in view of U.S. Patent No. 4,427,935 (Bowden). Claim 12 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang et al. and Forbes et al. as applied to claims 6-9 above, and further in view of U.S. Patent No. 4,427,935 (Bowden).

In rejecting claims 6-9, the Examiner asserted that Tang et al. teach the feature "controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value", as recited in claim 6. However, as discussed above, Tang et al. do not teach or suggest such a feature. Instead, the saturation current value, according to Tang et al., varies according to the supply voltage. As correctly pointed out by the Examiner, Tang et al. also fail to teach "the substrate potential control circuit" which includes various components as recited in claim 6. The Examiner asserted that Forbes et al. disclose the features associated with the substrate potential

control circuit. The Applicants respectfully submit that Forbes et al. do not disclose controlling the substrate potential of a MOS transistor "so that an actual saturation current value of the MOS transistor is equal to a target saturation current value", as recited in claim 6.

According to MPEP §2142, to establish a prima facie case of obviousness, there must be some suggestion or motivation to modify the reference or to combine reference teachings. The Applicants respectfully submit that there is no motivation in Tang et al. that suggests a combination with Forbes et al. In addition, even if Tang et al. and Forbes et al. are combined, the Applicants respectfully submit that the combination does not remedy the deficiency of Tang et al. because the Examiner cited Forbes et al. to remedy a different feature than "controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value", which is recited in claim 6. That is, the Examiner failed to establish a prima facie case of obviousness. Therefore, claim 6 is not obvious over Tang et al. in view of Forbes et al. The Applicants respectfully request that rejection of claim 6 based on obviousness be withdrawn.

Claims 7-12 depend from claim 6. Therefore, claims 7-12 are patentable at least for the reasons stated above with respect to claim 6 and for the additional features recited therein. The Applicants respectfully request that rejection to claims 7-12 based on obviousness be withdrawn.

By this Amendment, all rejections raised in the Office Action have been overcome. Therefore, it is believed that all pending claims are now in condition for allowance. Applicant therefore respectfully requests an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicant's representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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